5G: CMOS Low Noise Amplifier Design

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Abstract—The low-noise amplifier (LNA) is a vital component in wireless receiver systems, as it amplifies extremely weak signals received from the antenna while adding minimal noise and distortion. In this work, a CMOS-based LNA with an intended operating frequency of 26 GHz is designed for 5G millimeter-wave applications. Because of its small size, low power consumption, and suitability for large-scale integration, CMOS technology was chosen. To ensure dependable operation, the design must overcome obstacles like parasitic effects, device noise, and stability problems at such high frequencies through careful transistor sizing, bias optimization, and the application of matching and stabilization techniques. Advanced Design System (ADS) software is used to design and simulate the circuit, allowing for precise RF modeling and S-parameter evaluation. The LNA achieves a forward gain (S_{21}) of 11.16 dB at 26 GHz, indicating effective signal amplification at the target frequency, according to measurement and simulation results. Optimal reflection coefficient values of S_{11} = 58.558 – j41.767 and S_{22} = 78.449 – j44.026 are obtained by implementing input and output impedance matching networks to reduce reflections and maximize power transfer. The findings verify that the suggested CMOS LNA is appropriate for front-end 5G receiver applications and offers a solid foundation for additional performance improvement in subsequent designs.

Index Terms—*Low Noise Amplifier, 5G, Gain, Impedance Matching, Advanced Design System.*

I. INTRODUCTION

Since it significantly affects the system's overall sensitivity and noise performance, the low-noise amplifier (LNA) is the first and most important component in a wireless receiver's radio frequency (RF) front-end. Its main purpose is to boost very weak signals that the antenna receives, usually in

the range of –100 dBm (or very small voltage levels), up to usable voltage levels like 0.5 V to 1 V without noticeably lowering the signal-to-noise ratio. The LNA has a significant impact on the receiver's gain and overall noise figure due to its advantageous location at the front of the receiver chain.

ISM band radios, wireless local area networks (WLANs), GPS receivers, satellite communication systems, and cellular communication devices are just a few of the many wireless applications that make extensive use of low-noise amplifiers. The LNA in each of these systems needs to produce enough gain with the least amount of noise. The Friis equation, which demonstrates that raising the first amplification stage's gain and lowering its noise figure greatly enhances the receiver's overall performance, can be used to analyze and optimize the LNA's performance. Thus, one of the main design objectives in LNA development is to achieve high gain and low noise figure.

The performance requirements for transceivers have significantly increased due to the quick development of 5G wireless communication, particularly for millimetre-wave (mm-wave) frequency bands. Large bandwidths and high data rates are provided by mm-wave systems, but they also confront significant technological obstacles like a short coverage range, high path loss, higher power consumption, and decreased system reliability. Front-end components like the LNA, which must sustain steady, low-noise operation at extremely high frequencies, are subject to stringent requirements as a result of these difficulties.

Millimetre-wave communication systems have traditionally employed III–V compound semiconductor technologies, such as gallium arsenide (GaAs), because of their superior high-frequency performance. Due to their superior high-frequency performance, III–V compound semiconductor technologies like gallium arsenide (GaAs) have historically been used in millimetre-wave communication systems. However, high-frequency RF circuits can now be designed with better integration capabilities, smaller chip areas, and lower costs thanks to advancements in CMOS technology. CMOS is a practical and affordable option for implementing LNAs in modern 5G systems because modern nanoscale CMOS processes offer enough transistor speed and performance to support mm-wave applications.

A typical low-noise amplifier consists of a transistor with three main terminals: gate, source, and drain. The transistor is connected to an input matching network, an output matching network, and a biasing circuit to ensure proper operating conditions. The input matching network is used to match the amplifier’s input impedance to the antenna or source impedance for maximum power transfer and minimum reflection, while the output matching network ensures efficient power delivery to the subsequent stage. The biasing circuit stabilizes the operating point of the transistor, enabling consistent and reliable amplification performance across varying conditions.

II. LITERATURE SURVEY:

Literature review based on various research papers

P.Chandrasekhar,B.Raghuveer[1]

GaAs pHEMT technology has been used to design an LNA that operates in the 25 GHz band with a maximum gain of 26.74 dB and a minimum noise figure of 1.67 dB.

Kusuma M.S, Rajendra Chikkanagouda[2]
In this paper, a cascaded four-stage Common Source (CS) amplifier Low Noise Amplifier (LNA) circuit based on 65 nm CMOS technology is designed to function in the frequency range of (57-86 GHz).

Rashmi hazarika, manash pratim sharmav[3]
Here achieves a gain of 15.17dB with substantial enhancement of linearity.The peak gain is achieved at 3.5GHz.

Anjana Jyothi Banu,Dr.G.Kavya, D.Jahnavi[4]
This presents a design of low noise amplifier for 5G applications based on 180nm CMOS technology.LNA is designed to operate at 26 GHz in the K-band.

M. Ramana Reddy [5]
The proposed GaAs pHEMT process of wideband LNAis performed and evaluated at 50nm using current reuse Topology.

III. PROPOSED SYSTEM

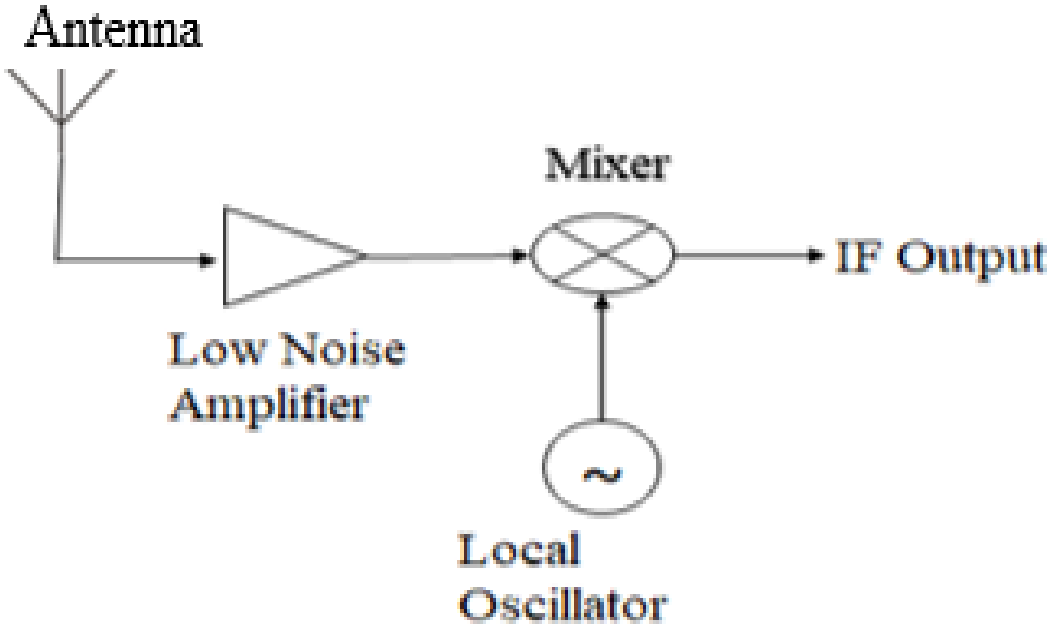

Fig 1: Rf Reciever

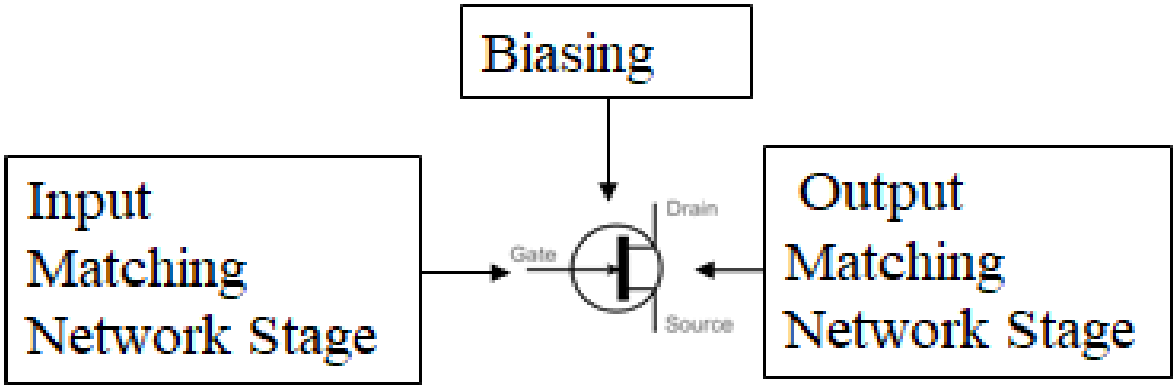

Fig 2: LNA-Low Noise Amplifier

In this work LNA is designed to operate in 26 GHZ frequency. Using simulation software called Advanced Design System (ADS), the low noise amplifier was designed and tested. The ADS tool has a large library. The active device utilised in this work is from the S-parameter library. The device stability and other characteristics are obtained by the design using an S-parameter simulation controller. Moreover, harmonic balancing simulation has been utilised to observe linearity.

In this study, low noise figure is attained using GaAs p-HEMT technology. The ATF-34143 serves as the amplifier's primary component. It is a Pseudomorphic High Electron Mobility Transistor with extremely low noise (p-HEMT). The key reason for choosing the ATF-34143 device for this project is that it has a very low noise resistance, which makes it much simpler to construct a low noise amplifier by reducing the sensitivity of noise performance caused by differences in input and bias the circuit. impedance match. Inductors, capacitors and resistors are used in this design to provide input /output matching and biasing of the circuit.

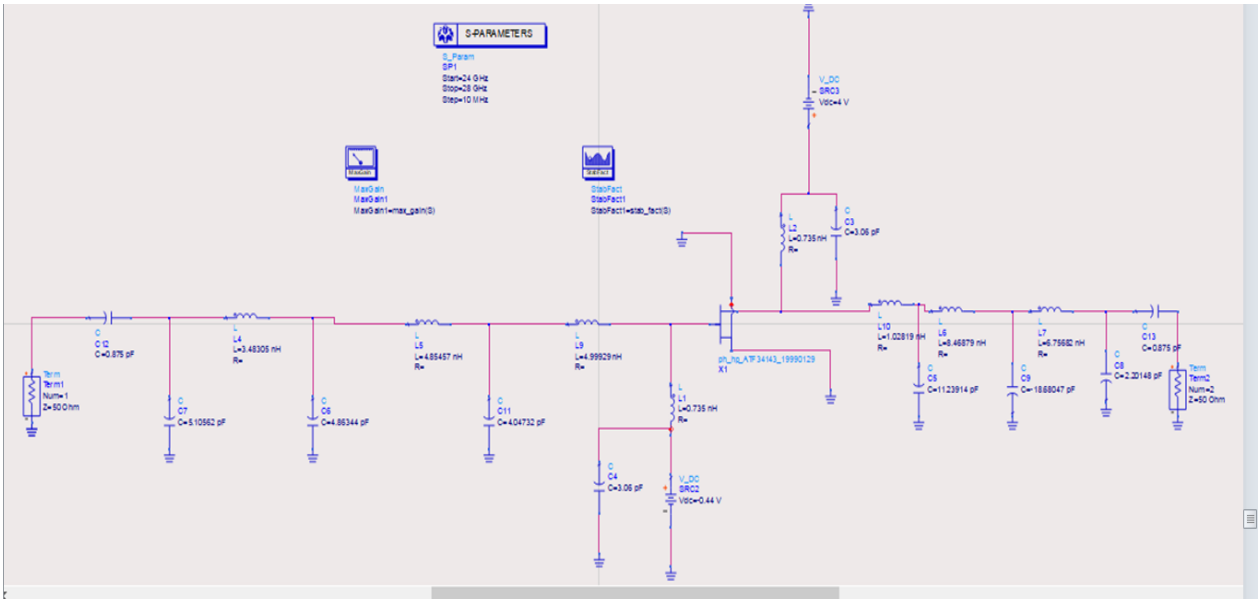

Fig 3: Circuit design of LNA

LNA's initial stage at input is designed using input matching network and output matching network.The supply voltage applied for this circuit is 4 V.

Design formulas:

1. Gain of LNA

Voltage gain:$A_v = \frac{V_{out}}{V_{in}}$ 1

Power gain (linear):$G = \frac{P_{out}}{P_{in}}$ 2

Power gain in decibels:$G_{dB} = 10log_{10}(G) = 20log_{10}\left(\frac{V_{out}}{V_{in}}\right)$ 3

Gain Parameters

- A_v– Voltage gain
- V_{out}– Output voltage
- V_{in}– Input voltage
- G– Power gain (linear)
- G_{dB}– Power gain in decibels
- P_{out}– Output power
- P_{in}– Input power

2. Noise Figure (NF)

Noise Factor:

$$F = \frac{(S/N)_{in}}{(S/N)_{out}} \quad (4)$$

Noise Figure in dB:

$$NF = 10log_{10}(F) \quad (5)$$

Noise Parameters

F– Noise factor (linear value of noise performance)

NF– Noise figure (noise factor expressed in decibels)

S/N_{in}– Signal-to-noise ratio at input

S/N_{out}– Signal-to-noise ratio at output

3. Friis Formula for Cascaded Noise Figure

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \quad (6)$$

Friis Formula Terms

$F_1, F_2, F_3, \ldots$– Noise factors of each amplifier stage

$G_1, G_2, G_3, \ldots$– Linear gains of each stage

4. Input Reflection Coefficient (S_{11})

$$\Gamma_{in} = \frac{Z_{in}-Z_0}{Z_{in}+Z_0} \quad 7$$

Return loss:

$$RL = -20log_{10} | \Gamma_{in} | \quad 8$$

S-Parameters and Reflection Coefficients

S_{11}– Input reflection coefficient (input return loss parameter)
S_{22}– Output reflection coefficient (output return loss parameter)
S_{21}– Forward transmission coefficient (forward gain parameter)
S_{12}– Reverse transmission coefficient (reverse isolation parameter)
Γ_{in}– Input reflection coefficient
Γ_{out}– Output reflection coefficient
Z_{in}– Input impedance of the amplifier
Z_{out}– Output impedance of the amplifier
Z_0– Characteristic impedance (usually 50 Ω)

5. Output Reflection Coefficient (S_{22})

$$\Gamma_{out} = \frac{Z_{out}-Z_0}{Z_{out}+Z_0} \quad 9$$

6. Impedance Matching Condition

For maximum power transfer:

$$Z_{in} = Z_0 and Z_{out} = Z_0 \quad 10$$

Where $Z_0$is usually 50 Ω.

7.Transconductance (MOSFET used in LNA)

$$g_m = \frac{2I_D}{V_{GS}-V_{TH}} \quad 11$$

MOSFET / CMOS Parameters

g_m– Transconductance of the transistor
I_D– Drain current
V_{GS}– Gate-to-source voltage
V_{TH}– Threshold voltage of the MOSFET
V_{ov}– Overdrive voltage ($V_{GS} - V_{TH}$)

8.Input Impedance of Common Source LNA

$$Z_{in} \approx j\omega L_g + \frac{1}{j\omega C_{gs}} + g_m L_s \quad 12$$

Frequency and Reactive Elements
ω– Angular frequency ($\omega = 2\pi f$)
f– Operating frequency
L_g– Gate inductance
L_s– Source inductance
C_{gs}– Gate-to-source capacitance

IV. SIMULATION RESULTS

The designed low noise amplifier circuit as shown in Fig.3 has simulated and analysed with the help of ADS tool. First, we need to check whether the circuit is unconditionally stable or not. For the circuit to be unconditionally stable K >1 and |Δ|<1.
Were,

$$K = (1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2)/(2|S_{21}||S_{12}|) \quad (13)$$

$$\Delta = S_{11}S_{22} - S_{21}S_{12} \quad (14)$$

Stability Parameters

- K– Rollet's stability factor
- Δ– Determinant of the S-parameter matrix

The simulation result for stability factor of designed LNA is shown in fig.4. The result indicates that the LNA is stable as the stability factor is equal to 1.

Fig 4: Stability factor of LNA

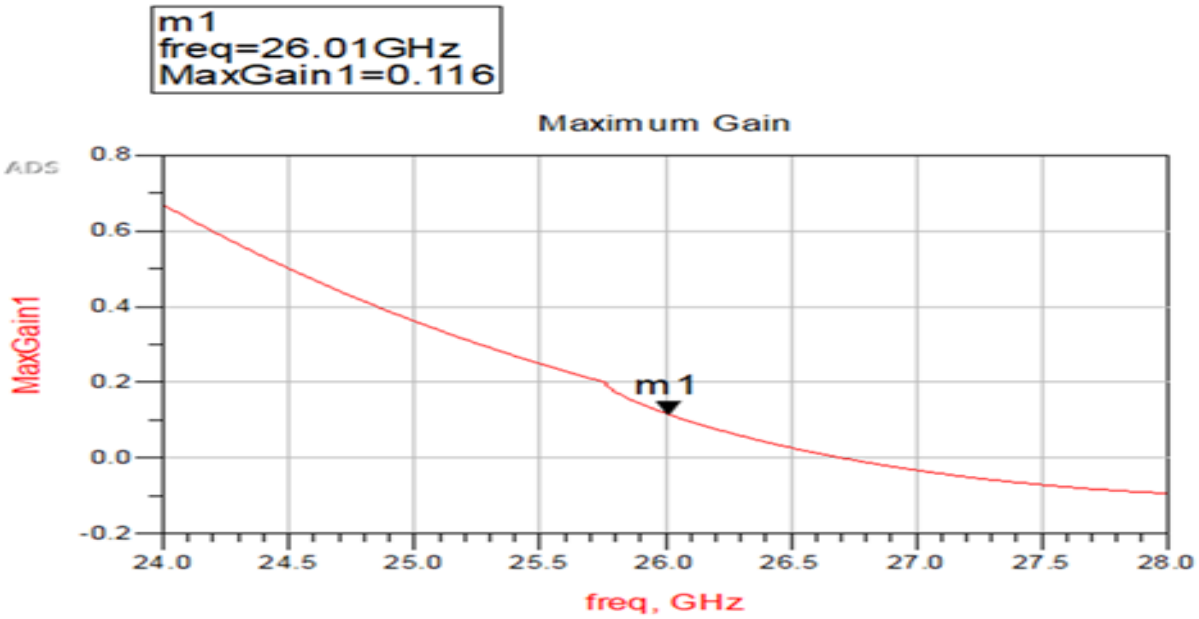

Fig 5: Gain of LNA

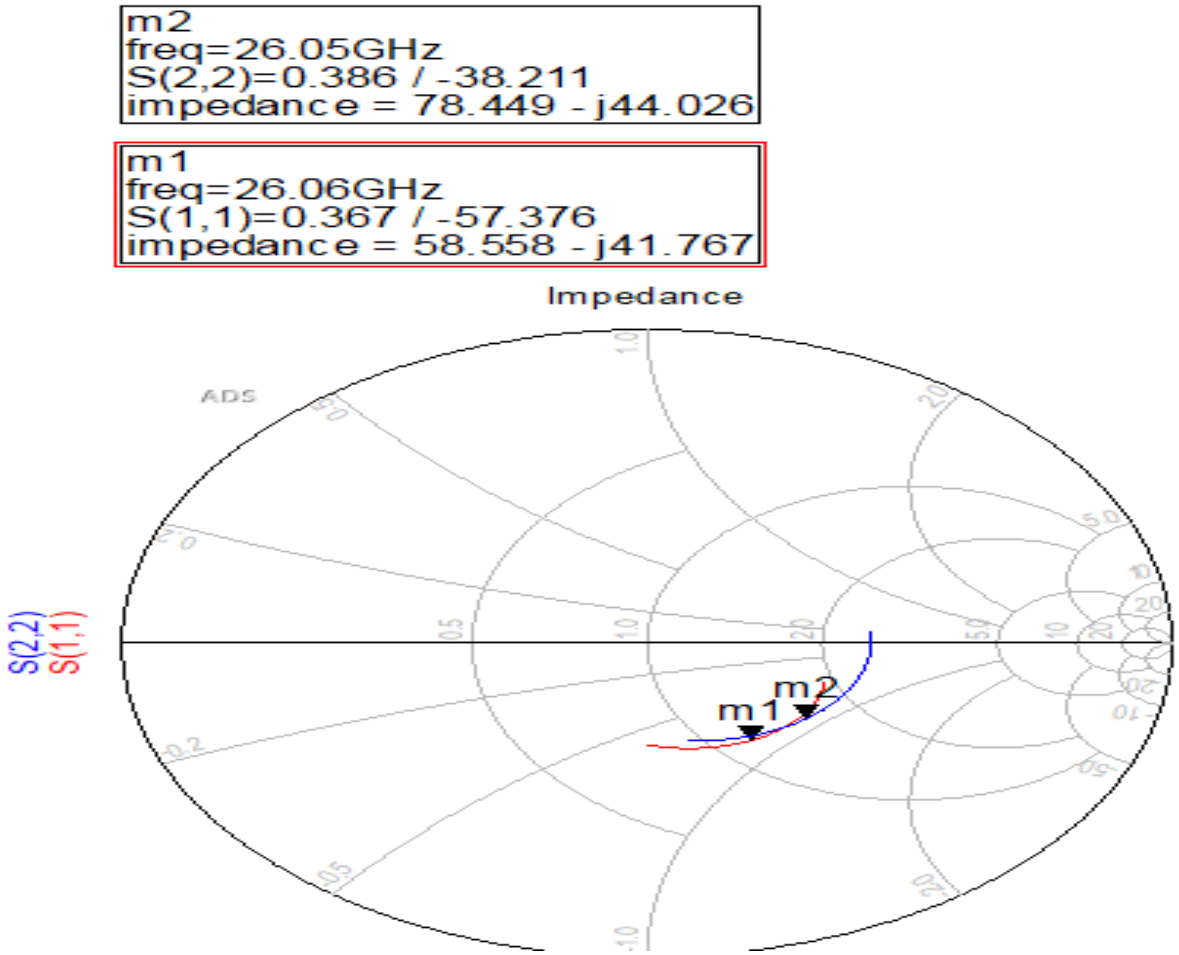

Fig 6: Input and Output Impedance

The above figure shows the simulation output of input impedance S11 is 58.558 - j41.767 and the simulation output of output impedance impedance is 78.449 – j44.026 in 26 GHZ band.

V. CONCLUSION

In this paper, the design of CMOS LNA operated in 26 GHz band has been presented. It is observed that designed circuits are unconditionally stable. The power supply applied to the circuit is 4 V. The simulation results show that gain of 11.16 dB in the required 26 GHz band is obtained at 26 GHz.

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